

32GB DDR4-3200 U-DIMM 1.35V

288pin PC4-25600 DDR4 U-DIMM Non-ECC

(JUHOR) 玖合

Embedded
Storage
Solutions

32GB DDR4-3200^{XMP} U-DIMM 1.35V

288pin PC4-25600 DDR4 Unbuffered DIMM Non-ECC

Description

JUHOR 32G is a DDR4 3200 Mbps U-DIMM high-speed memory module that use 16pcs of 2Gx8bits, 8pcs of 4Gx8bits

DDR4 SDRAM in FBGA package and a 4Kbits

serial EEPROM on a 288-pin printed circuit board.

This JUHOR product is a Dual In-Line Memory Module and is intended for mounting into 288-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operation frequencies, programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

Features

- RoHS compliant products.
- JEDEC standard/ XMP2.0 standard Power supply
VDDQ= 1.35V (OC mode)
- VPP = 2.5V +0.25V / -0.125V
- Data transfer rates: PC4-25600
Programmable CAS Latency:
CL= 18
- 8 bit pre-fetch
- Burst Length (BL) switch on-the-fly BL8 or BC4
- Bi-directional Differential Data-Strobe
- On Die Termination, Nominal, Park, and Dynamic ODT
- Serial presence detect with EEPROM
Asynchronous reset
- Anti - sulfur resistor used
- Used for intel specially
- Operating Temperature(0°C ~ 85 °C)

Pin Identification

Symbol	Function
A0~A17 ₁ , BA0~BA1	Address/Bank input

DQ0~DQ63	Bi-direction data bus.
DQS0_t~DQS17_t	Data Buffer data strobes
DQS0_c~DQS17_c	Data Buffer data strobes
CK0_t, CK1_t	Register clock input
CK0_c, CK1_c	Register clocks input
ODT0 & ODT1	On-die termination control line
CS0_n~CS3_n	DIMM Rank Select Lines input.
RAS_n ²	Row address strobe
CAS_n ³	Column address strobe
WE_n ⁴	Write Enable
DM0~DM7	Data masks/high data strobes
VDD	Core power supply
VDDQ	I/O driver power supply
VREFCA	Command/address reference supply
VDDSPD	SPD EEPROM power supply
SA0~SA2	I2C serial bus address select for EEPROM
SCL	I2C serial bus clock for EEPROM
SDA	I2C serial bus data for EEPROM
VSS	Ground
RESET_n	Set DRAMs Known State
VTT	DRAM I/O termination supply
VPP	SDRAM Supply
ALERT_n	Register ALERT_n output
EVENT_n	SPD signals a thermal event has occurred
RFU	Reserved for future use

1. Address A17 is only valid for 16Gb x8 based SDRAMs.

2. RAS_n is a multiplexed function with A16.

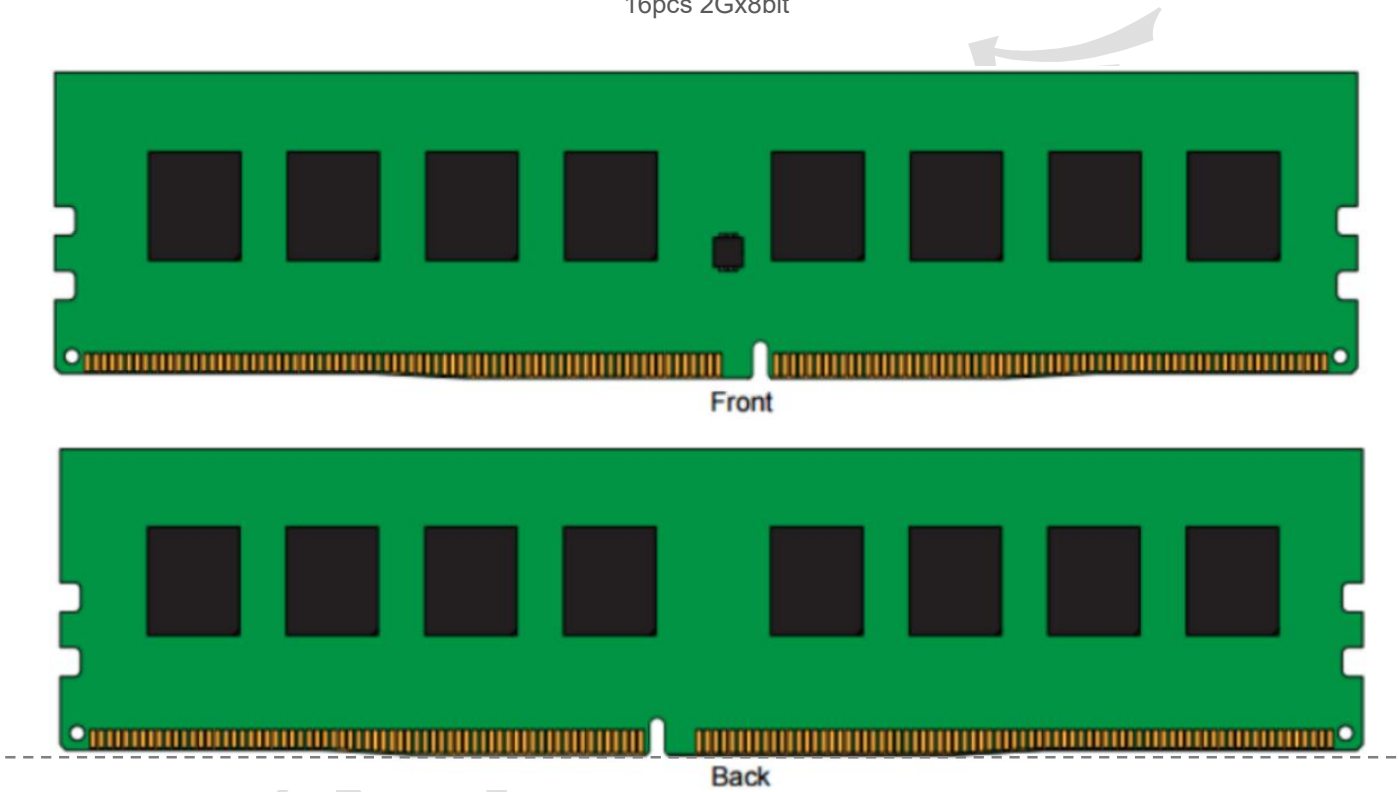
3. CAS_n is a multiplexed function with A15.

4. WE_n is a multiplexed function with A14.

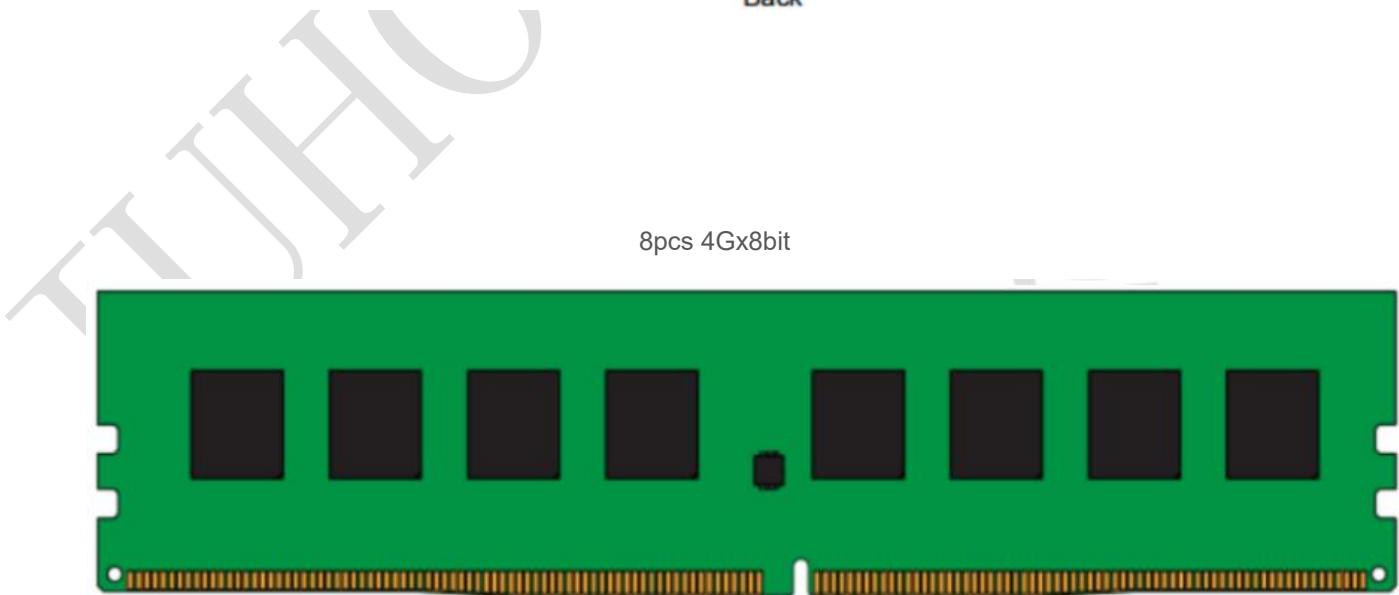
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Dimensions (Unit: millimeter)

16pcs 2Gx8bit



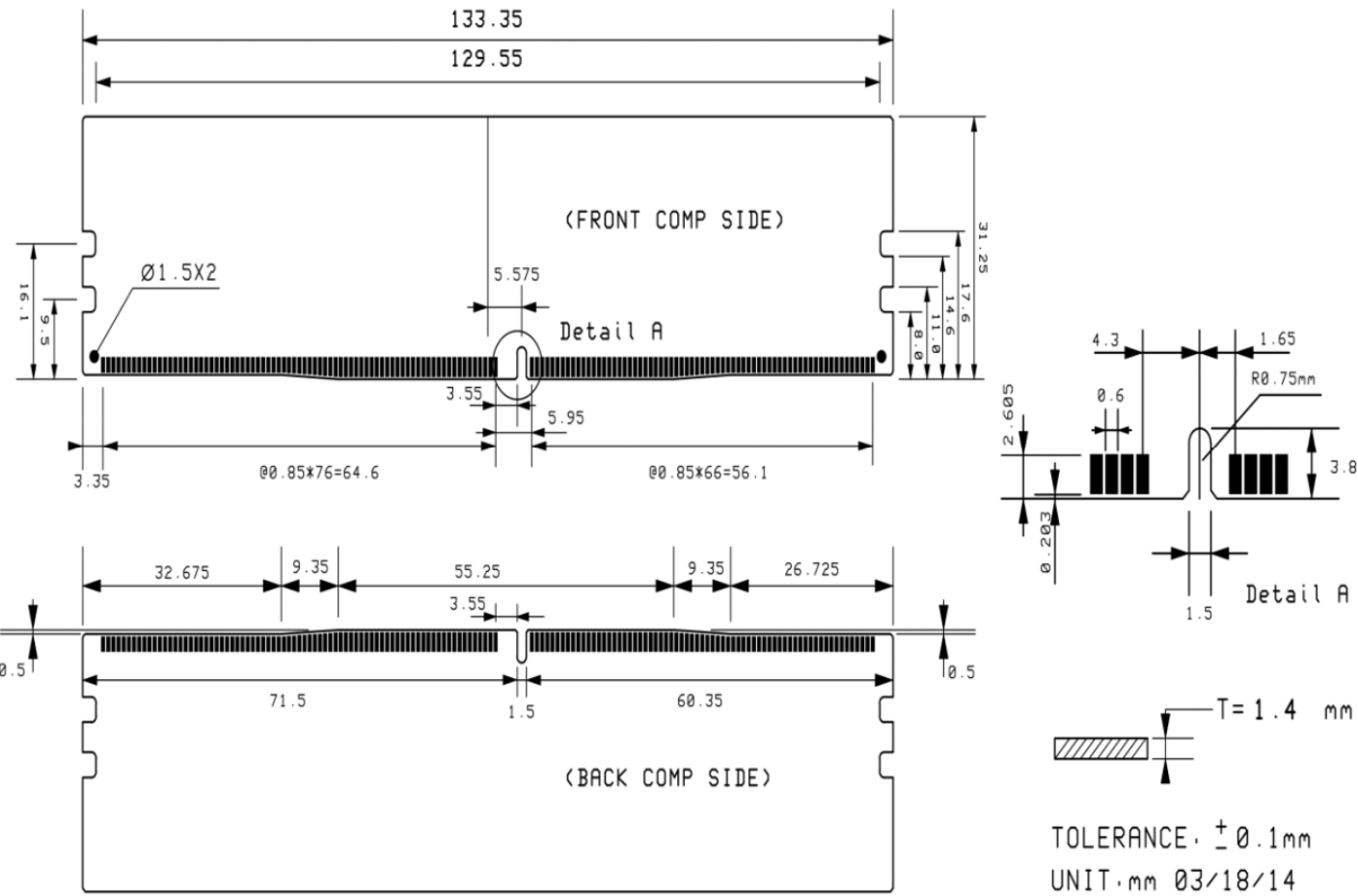
8pcs 4Gx8bit



Datasheet

JUHOR 玖合

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Note:1. Tolerances on all dimensions +/-0.1mm unless otherwise specified.

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Pin Assignments

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	NC	49	NC	97	DQ32	145	NC	193	GND	241	GND
2	GND	50	GND	98	GND	146	VREFCA	194	NC	242	DQ33
3	DQ04	51	NC	99	DM4_N	147	GND	195	GND	243	GND
4	GND	52	NC	100	NC	148	DQ05	196	NC	244	DQS4_C
5	DQ00	53	GND	101	GND	149	GND	197	NC	245	DQS4_T
6	GND	54	NC	102	DQ38	150	DQ01	198	GND	246	GND
7	DM0_N	55	GND	103	GND	151	GND	199	NC	247	DQ39
8	NC	56	NC	104	DQ34	152	DQS0_C	200	GND	248	GND
9	GND	57	GND	105	GND	153	DQS0_T	201	NC	249	DQ35
10	DQ06	58	RST_N	106	DQ44	154	GND	202	GND	250	GND
11	GND	59	VDD	107	GND	155	DQ07	203	CKE1	251	DQ45
12	DQ02	60	CKE0	108	DQ40	156	GND	204	VDD	252	GND
13	GND	61	VDD	109	GND	157	DQ03	205	NC	253	DQ41
14	DQ12	62	ACT_N	110	DM5_N	158	GND	206	VDD	254	GND
15	GND	63	BG0	111	NC	159	DQ13	207	BG1	255	DQS5_C
16	DQ08	64	VDD	112	GND	160	GND	208	ALERT_N	256	DQS5_T
17	GND	65	A12	113	DQ46	161	DQ09	209	VDD	257	GND
18	DM1_N	66	A09	114	GND	162	GND	210	A11	258	DQ47
19	NC	67	VDD	115	DQ42	163	DQS1_C	211	A07	259	GND
20	GND	68	A08	116	GND	164	DQS1_T	212	VDD	260	DQ43
21	DQ14	69	A06	117	DQ52	165	GND	213	A05	261	GND
22	GND	70	VDD	118	GND	166	DQ15	214	A04	262	DQ53
23	DQ10	71	A03	119	DQ48	167	GND	215	VDD	263	GND
24	GND	72	A01	120	GND	168	DQ11	216	A02	264	DQ49
25	DQ20	73	VDD	121	DM6_N	169	GND	217	VDD	265	GND
26	GND	74	CK0_T	122	NC	170	DQ21	218	CK1_T	266	DQS6_C
27	DQ16	75	CK0_C	123	GND	171	GND	219	CK1_C	267	DQS6_T
28	GND	76	VDD	124	DQ54	172	DQ17	220	VDD	268	GND
29	DM2_N	77	VTT	125	GND	173	GND	221	VTT	269	DQ55
30	NC	78	EVENT_N	126	DQ50	174	DQS2_C	222	PARITY	270	GND
31	GND	79	A00	127	GND	175	DQS2_T	223	VDD	271	DQ51
32	DQ22	80	VDD	128	DQ60	176	GND	224	BA1	272	GND
33	GND	81	BA0	129	GND	177	DQ23	225	A10	273	DQ61
34	DQ18	82	A16	130	DQ56	178	GND	226	VDD	274	GND
35	GND	83	VDD	131	GND	179	DQ19	227	NC	275	DQ57
36	DQ28	84	CS0_N	132	DM7_N	180	GND	228	A14	276	GND
37	GND	85	VDD	133	NC	181	DQ29	229	VDD	277	DQS7_C
38	DQ24	86	A15	134	GND	182	GND	230	NC	278	DQS7_T
39	GND	87	ODT0	135	DQ62	183	DQ25	231	VDD	279	GND
40	DM3_N	88	VDD	136	GND	184	GND	232	A13	280	DQ63
41	NC	89	CS1_N	137	DQ58	185	DQS3_C	233	VDD	281	GND
42	GND	90	VDD	138	GND	186	DQS3_T	234	NC	282	DQ59
43	DQ30	91	ODT1	139	SA0	187	GND	235	NC	283	GND
44	GND	92	VDD	140	SA1	188	DQ31	236	VDD	284	VDDSPD
45	DQ26	93	NC	141	SCL	189	GND	237	NC	285	SDA
46	GND	94	GND	142	VPP	190	DQ27	238	SA2	286	VPP
47	NC	95	DQ36	143	VPP	191	GND	239	GND	287	VPP
48	GND	96	GND	144	NC	192	NC	240	DQ37	288	VPP

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32GB, 2Gx8 Module (2 Rank x8)

32GB, 4Gx8 Module (1 Rank x8)

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- This technical information is based on industry standard data and tests believed to be reliable. However, JUHOR makes no warranties, either expressed or implied, as to its accuracy and assume no liability in connection with the use of this product. JUHOR reserves the right to make changes in specifications at any time without prior notice.

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Operating Temperature Condition

Parameter	Symbol	Rating	Unit	Note
Operating Temperature	TOPER	0 to 85	°C	1,2

Note: Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

Absolute Maximum DC Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on VDD relative to Vss	VDD	-0.3 ~ 1.5	V	1
Voltage on VDDQ pin relative to Vss	VDDQ	-0.3 ~ 1.5	V	1
Voltage on any pin relative to Vss	VIN, VOUT	-0.3 ~ 1.5	V	1
Storage temperature	TSTG	-55~+100	°C	1,2

Note: 1. Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

AC & DC Operating Conditions

Recommended DC operating conditions (Default mode)

Parameter	Symbol	Voltage	Rating			Unit	Notes
			Min	Typ.	Max		
Supply voltage	VDD	1.2V	1.14	1.2	1.26	V	1,2,3
Supply voltage for Output	VDDQ	1.2V	1.14	1.2	1.26	V	1,2,3
I/O Reference Voltage (DQ)	VREF _{DQ} (DC)	1.2V	0.49*VDD	0.50*VDD	0.51*VDD	V	4
I/O Reference Voltage (CMD/ADD)	VREF _{CA} (DC)	1.2V	0.49*VDD	0.50*VDD	0.51*VDD	V	4
AC Input Logic High	VIH(AC)	1.2V	VREF+100	-	VDD ²	mV	
AC Input Logic Low	VIL(AC)	1.2V	VSS ²	-	VREF-100	mV	
DC Input Logic High	VIH(DC)	1.2V	VREF+75	-	VDD	mV	
DC Input Logic Low	VIL(DC)	1.2V	VSS	-	VREF-75	mV	

Note: (1) Under all conditions VDDQ must be less than or equal to VDD.
(2) VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
(3) The DC bandwidth is limited to 200MHz.
(4) The AC peak noise on VREF may not allow VREF to deviate from VREF(DC) by more than ±1% VDD (for reference: approx. ±12mV)

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IDD Specification parameters Definition - 32GB

Parameter	Symbol	DDR4 3200 CL18	Unit
One bank ACTIVATE-PRECHARGE current	IDD0 ¹	304	mA
One bank ACTIVATE-PRECHARGE, wordline boost, IPP current	IPP0 ¹	48	mA
One Bank Active-Read-Precharge Current	IDD1 ¹	384	mA
Precharge Standby Current	IDD2N ²	216	mA
Precharge standby ODT current	IDD2NT ¹	256	mA
Precharge Power-Down Current	IDD2P ²	144	mA
Precharge Quiet Standby Current	IDD2Q ²	176	mA
Active standby current	IDD3N ²	360	mA
Active standby IPP current	IPP3N ²	120	mA
Active Power-Down Current	IDD3P ²	296	mA
Burst Read Current	IDD4R ¹	992	mA
Burst write current	IDD4W ¹	960	mA
Burst refresh current (1x REF)	IDD5B ¹	1568	mA
Burst refresh IPP current (1x REF)	IPP5B ¹	520	mA
Self refresh current: Normal temperature range (0–85°C)	IDD6N ²	176	mA
Self refresh current: Extended temperature range (0–95°C)	IDD6E ²	224	mA
Bank interleave read current	IDD7 ¹	1216	mA
Bank interleave read IPP current	IPP7 ¹	152	mA
Maximum power-down current	IDD8 ²	96	mA

Note: 1. One module rank in the active IDD/PP, the other rank in IDD2P/PP3N.
2. All ranks in this IDD/PP condition.
3. IDD current measure method and detail patterns are described on DDR4 component datasheet.
Only for reference.

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■ Timing Parameters & Specifications

Speed		DDR4-1866		DDR4-2133		DDR4-2400		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Clock Timing									
Minimum Clock Cycle Time (DLL off mode)	tCK (DLL OFF)	8	-	8	-	8	20	ns	22
Average Clock Period	tCK(avg)	1.071	<1.25	0.938	<1.071	0.833	<0.938	ps	35,36
Average high pulse width	tCH(avg)	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	
Average low pulse width	tCL(avg)	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	
Absolute Clock Period	tCK(abs)	tCK(avg)min + tJIT(per)min_to t	tCK(avg)max + tJIT(per)m ax_tot	tCK(avg)min + tJIT(per)min_to t	tCK(avg)max + tJIT(per)m ax_tot	tCK(avg)min + tJIT(per)min_to t	tCK(avg)max + tJIT(per)m ax_tot	tCK(avg)	
Absolute clock HIGH pulse width	tCH(abs)	0.45	-	0.45	-	0.45	-	tCK(avg)	23
Absolute clock LOW pulse width	tCL(abs)	0.45	-	0.45	-	0.45	-	tCK(avg)	24
Clock Period Jitter- total	JIT(per)_tot	-54	54	-0.1	0.1	-42	42	ps	23
Clock Period Jitter- deterministic	JIT(per)_dj	-27	27	TBD	TBD	-21	21	ps	26
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-43	43	TBD	TBD	-33	33	ps	
Cycle to Cycle Period Jitter	tJIT(cc)_total	107		94		83		ps	25
Cycle to Cycle Period Jitter deterministic	tJIT(cc)_dj	54		47		42		ps	26
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	86		75		67		ps	
Duty Cycle Jitter	tJIT(duty)	TBD	TBD	TBD	TBD	TBD	TBD	ps	
Cumulative error across 2 cycles	tERR(2per)	-79	79	-69	69	-61	61	ps	
Cumulative error across 3 cycles	tERR(3per)	-94	94	-82	82	-73	73	ps	
Cumulative error across 4 cycles	tERR(4per)	-104	104	-91	91	-81	81	ps	
Cumulative error across 5 cycles	tERR(5per)	-112	112	-98	98	-87	87	ps	
Cumulative error across 6 cycles	tERR(6per)	-119	119	-104	104	-92	92	ps	
Cumulative error across 7 cycles	tERR(7per)	-124	124	-109	109	-97	97	ps	
Cumulative error across 8 cycles	tERR(8per)	-129	129	-113	113	-101	101	ps	
Cumulative error across 9 cycles	tERR(9per)	-134	134	-117	117	-104	104	ps	
Cumulative error across 10 cycles	tERR(10per)	-137	137	-120	120	-107	107	ps	
Cumulative error across 11 cycles	tERR(11per)	-141	141	-123	123	-110	110	ps	
Cumulative error across 12 cycles	tERR(12per)	-144	144	-126	126	-112	112	ps	
Cumulative error across 13 cycles	tERR(13per)	-147	147	-129	129	-114	114	ps	
Cumulative error across 14 cycles	tERR(14per)	-150	150	-131	131	-116	116	ps	
Cumulative error across 15 cycles	tERR(15per)	-152	152	-133	133	-118	118	ps	
Cumulative error across 16 cycles	tERR(16per)	-155	155	-135	135	-120	120	ps	
Cumulative error across 17 cycles	tERR(17per)	-157	157	-137	137	-122	122	ps	
Cumulative error across 18 cycles	tERR(18per)	-159	159	-139	139	-124	124	ps	
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR(nper)	tERR(nper)min = ((1 + 0.68ln(n)) * tJIT(per)_total min) tERR(nper)max = ((1 + 0.68ln(n)) * tJIT(per)_total max)						ps	
Command and Address setup time to CK_t, CK_c referenced to Vih(ac) / Vil(ac) levels	tIS(base)	100	-	80	-	62	-	ps	
Command and Address setup time to CK_t, CK_c referenced to Vref levels	tIS(Vref)	200	-	180	-	162	-	ps	
Command and Address hold time to CK_t, CK_c referenced to Vih(dc) / Vil(dc) levels	tIH(base)	125	-	105	-	87	-	ps	
Command and Address hold time to CK_t, CK_c referenced to Vref levels	tIH(Vref)	200	-	180	-	162	-	ps	
Control and Address Input pulse width for each input	tIPW	525	-	460	-	410	-	ps	
Command and Address Timing									
CAS_n to CAS_n command delay for same bank group	tCCD_L	max(5 nCK, 6.250 ns)	-	max(5 nCK, 6.250 ns)	-	max(5 nCK, 6.250 ns)	-	nCK	34
CAS_n to CAS_n command delay for different bank group	tCCD_S	4	-	4	-	4	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(2K)	Max(4nCK, 5.3ns)	-	Max(4nCK, 5.3ns)	-	Max(4nCK, 5.3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 1KB page size	tRRD_S(1K)	Max(4nCK, 4.2ns)	-	Max(4nCK, 3.7ns)	-	Max(4nCK, 3.3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 1/2KB page size	tRRD_S(1/2K)	Max(4nCK, 4.2ns)	-	Max(4nCK, 3.7ns)	-	Max(4nCK, 3.3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	tRRD_L(2K)	Max(4nCK, 6.4ns)	-	Max(4nCK, 6.4ns)	-	Max(4nCK, 6.4ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	tRRD_L(1K)	Max(4nCK, 5.3ns)	-	Max(4nCK, 5.3ns)	-	Max(4nCK, 4.9ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size	tRRD_L(1/2K)	Max(4nCK, 5.3ns)	-	Max(4nCK, 5.3ns)	-	Max(4nCK, 4.9ns)	-	nCK	34
Four activate window for 2KB page size	tFAW_2K	Max(28nCK, 3 0ns)	-	Max(28nCK, 3 0ns)	-	Max(28nCK, 3 0ns)	-	ns	34
Four activate window for 1KB page size	tFAW_1K	Max(20nCK, 2 3ns)	-	Max(20nCK, 2 1ns)	-	Max(20nCK, 2 1ns)	-	ns	34
Four activate window for 1/2KB page size	tFAW_1/2K	Max(16nCK, 1 7ns)	-	Max(16nCK, 1 5ns)	-	Max(16nCK, 1 3ns)	-	ns	34
Delay from start of internal write transaction to internal read command for different bank group	tWTR_S	max(2nCK, 2.5ns)	-	Max(28nCK, 30ns)	-	max(2nCK, 2.5ns)	-		1,2,e, 34
Delay from start of internal write transaction to internal read command for same bank group	tWTR_L	max(4nCK, 7.5ns)	-	Max(20nCK, 21ns)	-	max(4nCK, 7.5ns)	-		1,34
Internal READ Command to PRECHARGE Command delay	tRTP	max(4nCK, 7.5ns)	-	Max(16nCK, 13ns)	-	max(4nCK, 7.5ns)	-		
WRITE recovery time	tWR	15	-	15	-	15	-	ns	1

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Speed		DDR4-1866		DDR4-2133		DDR4-2400		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Write recovery time when CRC and DM are enabled	tWR_CRC_DM	tWR+max (5nCK,3.75ns)	-	tWR+max (5nCK,3.75ns)	-	tWR+max (5nCK,3.75ns)	-	ns	1, 28
delay from start of internal write transaction to internal read command for different bank group with both CRC and DM enabled	tWTR_S_C RC_DM	tWTR_S+max (5nCK,3.75ns)	-	tWTR_S+max (5nCK,3.75ns)	-	tWTR_S+max (5nCK,3.75ns)	-	ns	2, 29,34
delay from start of internal write transaction to internal read command for same bank group with both CRC and DM enabled	tWTR_L_C RC_DM	tWTR_L+max (5nCK,3.75ns)	-	tWTR_L+max (5nCK,3.75ns)	-	tWTR_L+max (5nCK,3.75ns)	-	ns	3,30,34
DLL locking time	tDLLK	597	-	768	-	768	-	nCK	
Mode Register Set command cycle time	tMRD	8	-	8	-	8	-	nCK	
Mode Register Set command update delay	tMOD	max(24nCK,15ns)	-	max(24nCK,15ns)	-	max(24nCK,15ns)	-	nCK	
Multi-Purpose Register Recovery Time	tMPRR	1	-	1	-	1	-	nCK	33
Multi Purpose Register Write Recovery Time	tWR_MPR	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-		
Auto precharge write recovery + precharge time	tDAL(min)	Programmed WR + roundup (tRP / tCK(avg))						nCK	
DQ0 or DQ10 driven to 0 set-up time to first DQS rising edge	tPDA_S	0.5	-	0.5	-	0.5	-	UI	45,47
DQ0 or DQ10 driven to 0 hold time from last DQS fall-ing edge	tPDA_H	0.5	-	0.5	-	0.5	-	UI	45,47
CS_n to Command Address Latency									
CS_n to Command Address Latency	tCAL	4	-	4	-	5	-	nCK	
DRAM Data Timing									
DQS_t,DQS_c to DQ skew, per group, per access	tDQSQ	-	0.16	-	0.16	-	0.16	tCK(avg)/2	13,18
DQ output hold time from DQS_t,DQS_c	tQH	0.76	-	0.76	-	0.76	-	tCK(avg)/2	13,17,18
Data Valid Window per device: tQH - tDQSQ for a device	tDVWd	0.63	-	0.64	-	0.64	-	UI	16,17,18
Data Valid Window per device, per pin: tQH - tDQSQ each device' s output	tDVWp	0.66	-	0.69	-	0.72	-	UI	16,17,18
Data Strobe Timing									
DQS_t, DQS_c differential READ Preamble	tRPRE	0.9	NOTE44	0.9	NOTE44	0.9	NOTE44	tCK	40
		NA	NA	NA	NA	1.8	NOTE44		
DQS_t, DQS_c differential READ Postamble	tRPST	0.33	TBD	0.33	TBD	0.33	TBD	tCK	41
DQS_t,DQS_c differential output high time	tQSH	0.4	-	0.4	-	0.4	-	tCK	
DQS_t,DQS_c differential output low time	tQSL	0.4	-	0.4	-	0.4	-	tCK	21
DQS_t, DQS_c differential WRITE Preamble	tWPRE	0.9	-	0.9	-	0.9	-	tCK	20
		NA	NA	NA	NA	1.8	NOTE44		
DQS_t, DQS_c differential WRITE Postamble	tWPST	0.33	TBD	0.33	TBD	0.33	TBD	tCK	42
DQS_t and DQS_c low-impedance time (Referenced from RL-1)	tLZ(DQS)	-390	195	-360	180	-300	150	tCK	43
DQS_t and DQS_c high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	195	-	180	-	150	tCK	
DQS_t, DQS_c differential input low pulse width	tDQSL	0.46	0.54	0.46	0.54	0.46	0.54	ps	
DQS_t, DQS_c differential input high pulse width	tDQSH	0.46	0.54	0.46	0.54	0.46	0.54	ps	
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (1 clock preamble)	tDQSS	-0.27	0.27	-0.27	0.27	-0.27	0.27	tCK	
DQS_t, DQS_c falling edge setup time to CK_t, CK_c rising edge	tDSS	0.18	-	0.18	-	0.18	-	tCK	
DQS_t, DQS_c falling edge hold time from CK_t, CK_c rising edge	tDSH	0.18	-	0.18	-	0.18	-	tCK	
DQS_t, DQS_c rising edge output timing locatino from rising CK_t, CK_c with DLL On mode	tDQSCK (DLL On)	-195	195	-180	180	-175	175	ps	37,38,39
DQS_t, DQS_c rising edge output variance window per DRAM	tDQSKI (DLL On)	-	330	-	310	-	290	ps	37,38,39
MPSM Timing									
Command path disable delay upon MPSM entry	tMPED	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-		
Valid clock requirement after MPSM entry	tCKMPE	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-		
Valid clock requirement before MPSM exit	tCKMPX	tCKSRX(min)	-	tCKSRX(min)	-	tCKSRX(min)	-		
Exit MPSM to commands not requiring a locked DLL	tXMP	txs(imin)	-	txs(imin)	-	txs(imin)	-		
Exit MPSM to commands requiring a locked DLL	tXMPDLL	tXMP(min) + tXSDLL(min)	-	tXMP(min) + tXSDLL(min)	-	tXMP(min) + tXSDLL(min)	-		
CS setup time to CKE	tMPX_S	tISmin + tIHmin	-	tISmin + tIHmin	-	tISmin + tIHmin	-		
Calibration Timing									
Power-up and RESET calibration time	tZQinit	1024	-	1024	-	1024	-	nCK	
Normal operation Full calibration time	tZQoper	512	-	512	-	512	-	nCK	
Normal operation Short calibration time	tZQCS	128	-	128	-	128	-	nCK	
Reset/Self Refresh Timing									
Exit Reset from CKE HIGH to a valid command	tXPR	max (5nCK,tRFC(min)+10ns)	-	max (5nCK,tRFC(min)+10ns)	-	max (5nCK,tRFC(min)+10ns)	-		
Exit Self Refresh to commands not requiring a locked DLL	tXS	tRFC(min)+10ns	-	tRFC(min)+10ns	-	tRFC(min)+10ns	-		
SRX to commands not requiring a locked DLL in Self Refresh ABORT	tXS_ABORT(min)	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-		
Exit Self Refresh to ZQCL,ZQCS and MRS (CL,CWL,WR,RTP and Gear Down)	tXS_FAST (min)	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-		

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Speed		DDR4-1866		DDR4-2133		DDR4-2400		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-		
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-		
Minimum CKE low width for Self refresh entry to exit timing with CA Parity enabled	tCKESR_PAR	tCKE(min)+1nCK+PL	-	tCKE(min)+1nCK+PL	-	tCKE(min)+1nCK+PL	-		
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	max(5nCK,10ns)	-	max(5nCK,10ns)	-	max(5nCK,10ns)	-		
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down when CA Parity is enabled	tCKSRE_PAR	max(5nCK,10ns)+PL	-	max(5nCK,10ns)+PL	-	max(5nCK,10ns)+PL	-		
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max(5nCK,10ns)	-	max(5nCK,10ns)	-	max(5nCK,10ns)	-		
Power Down Timing									
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max(4nCK,6ns)	-	max(4nCK,6ns)	-	max(4nCK,6ns)	-		
CKE minimum pulse width	tCKE	max(3nCK, 5ns)	-	max(3nCK, 5ns)	-	max(3nCK, 5ns)	-		31,32
Command pass disable delay	tCPDED	4	-	4	-	4	-	nCK	
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI		6
Timing of ACT command to Power Down entry	tACTPDEN	1	-	2	-	2	-	nCK	7
Timing of PRE or PREA command to Power Down entry	tPRPDEN	1	-	2	-	2	-	nCK	7
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL+4+1	-	RL+4+1	-	RL+4+1	-	nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL+4+(tWR/tCK(avg))	-	WL+4+(tWR/tCK(avg))	-	WL+4+(tWR/tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL+4+WR+1	-	WL+4+WR+1	-	WL+4+WR+1	-	nCK	5
Timing of WR command to Power Down entry (BC4MRS)	tWRPBC4DEN	WL+2+(tWR/tCK(avg))	-	WL+2+(tWR/tCK(avg))	-	WL+2+(tWR/tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BC4MRS)	tWRAPBC4DEN	WL+2+WR+1	-	WL+2+WR+1	-	WL+2+WR+1	-	nCK	5
Timing of REF command to Power Down entry	tREFPDEN	1	-	2	-	2	-	nCK	7
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-		
PDA Timing									
Mode Register Set command cycle time in PDA mode	tMRD_PDA	max(16nCK,10ns)		max(16nCK,10ns)		max(16nCK,10ns)			
Mode Register Set command update delay in PDA mode	tMOD_PDA	tMOD		tMOD		tMOD			
ODT Timing									
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONAS	1.0	9.0	1.0	9.0	1.0	9.0	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFAS	1.0	9.0	1.0	9.0	1.0	9.0	ns	
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)	
Write Leveling Timing									
First DQS_t/DQS_n rising edge after write leveling mode is programmed	tWLMRD	40	-	40	-	40	-	nCK	12
DQS_t/DQS_n delay after write leveling mode is programmed	tWLDQSEN	25	-	25	-	25	-	nCK	12
Write leveling setup time from rising CK_t, CK_c crossing to rising DQS_t/DQS_n crossing	tWLS	0.13	-	0.13	-	0.13	-	tCK(avg)	
Write leveling hold time from rising DQS_t/DQS_n crossing to rising CK_t, CK_c crossing	tWLH	0.13	-	0.13	-	0.13	-	tCK(avg)	
Write leveling output delay	tWLO	0	9.5	0	9.5	0	9.5	ns	
Write leveling output error	tWLOE							ns	
CA Parity Timing									
Commands not guaranteed to be executed during this time	tPAR_UNKNOWN	-	Max(2nCK,3ns)	-	Max(2nCK,3ns)	-	Max(2nCK,3ns)		
Delay from errant command to ALERT_n assertion	tPAR_ALERT_ON	-	PL+6ns	-	PL+6ns	-	PL+6ns		
Pulse width of ALERT_n signal when asserted	tPAR_ALERT_PW	56	112	64	128	72	144	nCK	
Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	tPAR_ALERT_RSP	-	50	-	57		64	nCK	
Parity Latency	PL	4		4		5		nCK	
CRC Error Reporting									
CRC error to ALERT_n latency	tCRC_ALERT	3	13	3	13	3	13	ns	
CRC ALERT_n pulse width	CRC_ALERT_PW	6	10	6	10	6	10	nCK	
tREFI									
tRFC1 (min)	2Gb	160	-	160	-	160	-	ns	
	4Gb	260	-	260	-	260	-	ns	
	8Gb	350	-	350	-	350	-	ns	
	16Gb	TBD	-	TBD	-	TBD	-	ns	
tRFC2 (min)	2Gb	110	-	110	-	110	-	ns	
	4Gb	160	-	160	-	160	-	ns	
	8Gb	260	-	260	-	260	-	ns	
	16Gb	TBD	-	TBD	-	TBD	-	ns	
tRFC4 (min)	2Gb	90	-	90	-	90	-	ns	
	4Gb	110	-	110	-	110	-	ns	
	8Gb	160	-	160	-	160	-	ns	
	16Gb	TBD	-	TBD	-	TBD	-	ns	

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SERIAL PRESENCE DETECT SPECIFICATION (Serial Presence Detect only for reference)

Byte	Function Described	Function	HEX Value
0	Number of Bytes Used / Number of Bytes in SPD Device / CRC Coverage	SPD Total: 512Bytes, SPD Used : 384Bytes	23
1	SPD Revision	Version 1.1	11
2	Key Byte / DRAM Device Type	DDR4 SDRAM	0C
3	Key Byte / Module Type	SO-DIMM	03
4	SDRAM Density and Banks	4 bank group / 4 bank	85
5	SDRAM Addressing	Row : 16	21
6	SDRAM Package Type	Mono / Not specified	00
7	SDRAM Optional Features	Unlimited MAC	08
8	SDRAM Thermal and Refresh Options	-	00
9	Other SDRAM Optional Features	Post package repair supported	40
10	Reserved	-	00
11	Module Nominal Voltage, VDD	1.2v	03
12	Module Organization	1Rank	01
13	Module Memory Bus Width	Non ECC	03
14	Module Thermal Sensor	Thermal Sensor included	80
15-16	Reserved	-	00
17	Timebases	MTB: 125ps	00
18	SDRAM Minimum Cycle Time (tCKAVGmin)	0.833 ns	07
19	SDRAM Maximum Cycle Time (tCKAVGmax)	1.5 ns	0C
20	CAS Latencies Supported, First Byte	CL 10,11,12,13,14	F8
21	CAS Latencies Supported, Second Byte	CL 15,16,17,18	0F
22	CAS Latencies Supported, Third Byte	-	00
23	CAS Latencies Supported, Fourth Byte	-	00
24	Minimum CAS Latency Time(tAmin)	13.75 ns	6E
25	Minimum RAS to CAS Delay Time (tRCDmin)	13.75 ns	6E
26	Minimum Row Precharge Delay Time (tRPmin)	13.75 ns	6E
27	Upper Nibbles for tRASmin and tRCmin	-	11
28	Minimum Active to Precharge Delay Time (tRASmin), Least Significant Byte	32 ns	00
29	Minimum Active to Active/Refresh Delay Time (tRCmin), Least Significant Byte	45.75 ns	6E
30	Minimum Refresh Recovery Delay Time (tRFC1min), Least Significant Byte	-	F0
31	Minimum Refresh Recovery Delay Time (tRFC1min), Most Significant Byte	350 ns	0A
32	Minimum Refresh Recovery Delay Time (tRFC2min), Least Significant Byte	-	20
33	Minimum Refresh Recovery Delay Time (tRFC2min), Most Significant Byte	260 ns	08
34	Minimum Refresh Recovery Delay Time (tRFC4min), Least Significant Byte	-	00
35	Minimum Refresh Recovery Delay Time (tRFC4min), Most Significant Byte	160 ns	05
36	Minimum Four Activate Window Time (tFAWmin), Most Significant Nibble	-	00
37	Minimum Four Activate Window Time (tFAWmin), Least Significant Byte	21 ns	A8
38	Minimum Activate to Activate Delay Time (tRRD_Smin), different bank group	3.3 ns	1B
39	Minimum Activate to Activate Delay Time (tRRD_Lmin), same bank group	4.9 ns	28
40	Minimum CAS to CAS Delay Time (tCCD_Lmin), same bank group	5 ns	28
41	Upper Nibble for tWRmin	15 ns	00
42	Minimum Write Recovery Time(tWRmin)	15 ns	78
43	Upper Nibbles for tWTRmin	2.5/7.5 ns	00
44	Minimum Write to Read Time(WTR_Smin) , different bank group	2.5 ns	14
45	Minimum Write to Read Time(WTR_Lmin) , same bank group	7.5 ns	3C
46-59	Reserved, Base Configuration Section	-	00
60	Connector to SDRAM Bit Mapping	DQ0, DQ1, DQ2, DQ3	0E
61	Connector to SDRAM Bit Mapping	DQ4, DQ5, DQ6, DQ7	2E
62	Connector to SDRAM Bit Mapping	DQ8, DQ9, DQ10, DQ11	2E
63	Connector to SDRAM Bit Mapping	DQ12, DQ13, DQ14, DQ15	04
64	Connector to SDRAM Bit Mapping	DQ16, DQ17, DQ18, DQ19	03
65	Connector to SDRAM Bit Mapping	DQ20, DQ21, DQ22, DQ23	23
66	Connector to SDRAM Bit Mapping	DQ24, DQ25, DQ26, DQ27	24
67	Connector to SDRAM Bit Mapping	DQ28, DQ29, DQ30, DQ31	04
68	Connector to SDRAM Bit Mapping	CB0-3	00
69	Connector to SDRAM Bit Mapping	CB4-7	00
70	Connector to SDRAM Bit Mapping	DQ32, DQ33, DQ34, DQ35	24
71	Connector to SDRAM Bit Mapping	DQ36, DQ37, DQ38, DQ39	04
72	Connector to SDRAM Bit Mapping	DQ40, DQ41, DQ42, DQ43	04
73	Connector to SDRAM Bit Mapping	DQ44, DQ45, DQ46, DQ47	24
74	Connector to SDRAM Bit Mapping	DQ48, DQ49, DQ50, DQ51	24
75	Connector to SDRAM Bit Mapping	DQ52, DQ53, DQ54, DQ55	04
76	Connector to SDRAM Bit Mapping	DQ56, DQ57, DQ58, DQ59	04

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Byte	Function Described	Function	HEX Value
77	Connector to SDRAM Bit Mapping	DO60, DO61, DO62, DO63	2E
78-116	Reserved, Base Configuration Section	-	00
117	Fine Offset for Minimum CAS to CAS Delay Time(tCCD_Lmin), same bank group	0ns	00
118	Fine Offset for Minimum Activate to Activate Delay Time(tRRD_Lmin), different bank group	-0.1ns	9C
119	Fine Offset for Minimum Activate to Activate Delay Time(tRRD_Smin), same bank group	-0.075ns	B5
120	Fine Offset for Minimum Activate to Activate/Refresh Delay Time(tRCmin)	0ns	00
121	Fine Offset for Minimum Row Precharge Delay Time(tRPmin)	0ns	00
122	Fine Offset for Minimum RAS to CAS Delay Time(tRCDmin)	0ns	00
123	Fine Offset for Minimum CAS Latency Time(tAmin)	0ns	00
124	Fine Offset for SDRAM Maximum Cycle Time(tCKAVGmax)	0ns	00
125	Fine Offset for SDRAM Minimum Cycle Time(tCKAVGmin)	-0.042ns	D6
126	Cyclical Redundancy Code for Base Configuration Section, LSB	CRC-CCITT(LOW)	49
127	Cyclical Redundancy Code for Base Configuration Section, MSB	CRC-CCITT(HIGH)	06
128	(Unbuffered): Raw Card Extension, Module Nominal Height	Revision 0 30.00 mm	0F
129	(Unbuffered): Module Maximum Thickness	-	11
130	(Unbuffered): Reference Raw Card Used	Raw Card A Revision 0	00
131	(Unbuffered): Address Mapping from Edge Connector to DRAM	Standard	00
132-253	(Unbuffered): Reserved	-	00
254	(Unbuffered): CRC for Module Specific Section, Least Significant Byte	CRC-CCITT(LOW)	45
255	(Unbuffered): CRC for Module Specific Section, Most Significant Byte	CRC-CCITT(HIGH)	AD
256-319	Hybrid Memory Architecture Specific Parameters	-	00
320	Module Manufacturer ID Code, LSB	ADATA	04
321	Module Manufacturer ID Code, MSB		CB
322	Module ID: Module Manufacturing Location	*Note: 1	-
323	Module ID: Module Manufacturing Date(Year)	*Note: 2	-
324	Module ID: Module Manufacturing Date(Week)	*Note: 3	-
325-328	Module ID: Module Serial Number	*Note: 4	-
329-348	Module Part Number	*Note: 5	-
349	Module Revision Code	-	00
350	SDRAM Manufacturer's JEDEC ID Code, LSB	Hynix	80
351	SDRAM Manufacturer's JEDEC ID Code, MSB		AD
352	DRAM Stepping	-	FF
353-381	Manufacturer's Specific Data	*Note: 6	-
382	Reserved	-	00
383	Reserved	-	00
384-511	End User Programmable	*Note: 7	-

- Note : 1. Byte 322 -- Manufacturing location by manufacturing location (00:Taiwan /01:China)
2. Byte 323 -- Module manufacturing date by year (YY).
3. Byte 324 -- Module manufacturing date by week (WW).
4. Bytes 325~328 -- Module Serial Number.
5. Bytes 329~348 -- Manufacturer Part Number by module part number , (Unused digits are coded as ASCII blanks (20h)).
6. Bytes 353~381 -- These bytes are undefined and can be used for JUHOR's own purpose. Digits are coded as 00h except the following:
- 6-1. Bytes 353~367 -- Manufacturer's Specific Data by working order number.
- 6-2. Bytes 368~381 -- Manufacturer's Specific Data by SPD naming number.
7. Bytes 384~511 -- These bytes are undefined and can be used for JUHOR's own purpose. Digits are coded as 00h except the following:
- 7-1. Bytes 384,385 -- The byte is coded as specified values.

JUHOR 玖合

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