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JHE4800U4016

16GB DDR5-4800 U-DIMM 1.1V

288pin PC4-38400 DDR5 Unbuffered U-DIMM Non-ECC

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400-628-0106

16GB: 2G x64 PC5-4800
DDR5 288-pin UDIMM

Revision History

Version	Description	Modifier	Date
1.0	First Release		

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Features

- 288-pin UDIMM
- Sideband access with I3C-basic/I2C support
- Two independent I/O sub channels for increased bandwidth
- Gold edge contacts
- Halogen-free
- Fly-by topology
- Terminated clock, control and command/address bus

Description

This specification defines the electrical and mechanical requirements for 288-pin, double data rate, synchronous DRAM, unbuffered memory modules (DDR5 SDRAM UDIMMs).

Product Family Attributes

Parameter	Options	Notes
DIMM organization	x64,	Two 32-bitsub-channels(non-ECC)
DIMM dimensions (nominal)	133.35mm x 31.25mm	Refer to Module Dimensions
Pin count	288	
DDR5 SDRAM densities supported	16Gb	82-ball FBGA package for x8 devices
Capacity	16GB	
DDR5 SDRAM width	x8,	
Data transfer rate	PC5-4800	Refer to Key Timing Parameters
Serialpresence detect hub with tem- perature sensor	1024 byte	
Voltage (external supply, nominal)	V_{IN_Bulk}: 5V	Bulk input DC supply voltage from system
Voltage (PMIC default output)	V_{DD}: 1.1V (-33mV / +67mV)	Supply voltage from PMIC
	V_{DDQ}: 1.1V (-33mV / +67mV)	I/O Supply voltage from PMIC
	V_{PP}: 1.8V (–54mV / +108mV)	Pump voltage from PMIC
	1.8V LDO output	From PMIC to HUB
	1.0V LDO output	
Interface	1.1V signaling	

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Ordering Information

Part Number	Speed			Organization	Power	Leads
Micron 2G8	DDR5-4800	PC5-4800	4800MHz (0.416ns @ CL = 40)	2Gx64	1.1V	Gold

Pin Description

Symbol	Type	I/O Level	Description
CK[1:0]_A_t, CK[1:0]_B_t, CK[1:0]_A_c, CK[1:0]_B_c	Input	V_{DDQ}	**SDRAM Clocks** CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CA[12:0]_A CA[12:0]_B	Input	V_{DDQ}	**Command/Address Inputs:** CA signals provide the command and address inputs according to the Command Truth Table. Note that because some commands are multi- cycle, the pins may not be interchanged between devices on the same bus. The address inputs also provide the op-code during MODE REGISTER SET commands. The DDR5 component CA13 pin is strapped (connected) to either V_{SS} or V_{DDQ} depending on the strapped state of MIR.
CS[1:0]_A CS[1:0]_B	Input	V_{DDQ}	**Chip Select:** All commands are masked when CS_n is registered HIGH. CS_n provides for external rank selection on systems with multiple ranks. CS_n is considered part of the command code. CS_n is also used to enter and exit the parts from power down mode and self refresh mode. While not in self refresh mode the CS_n input buffer operates with the same ODT and V_{REF} parameters as configured by the CA_ODT strap setting or mode register. When in self refresh, the CS_n is a CMOS rail-to-rail signal with DC HIGH and LOW at 80% and 20% of V_{DD}.
ALERT_n	Output	V_{DDQ}	**Alert:** If there is an error in CRC, then ALERT_n drives LOW for the period time interval and returns HIGH. During connectivity test mode, this pin functions as an input. Usage of this signal is system-dependent. In the case where this pin is not connected, ALERT_n must be bonded to V_{DDQ} on the system board.
RESET_n	CMOS Input	V_{DDQ}	**Active Low Asynchronous Reset:** Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail-to-rail signal with DC HIGH and LOW at 80% and 20% of V_{DDQ}.
PWR_GOOD	Input Output	V_{DDQ}	**Power Good Indicator:** Open drain output. The PMIC ensures this pin HIGH when VIN_Bulk input supply, as well as all enabled output buck regulators and all LDO regulators tolerance threshold is maintained as configured in the appropriate register. The PMIC drives this pin LOW when VIN_Bulk input goes below the threshold or when any of the enabled output buck regulator exceeds the thresholds configured in the appropriate register or when any LDO output regulator exceeds the threshold configured in the appropriate register. As an input, the PMIC disables its output regulator when this pin is LOW. The LDO outputs remain on.
HSCL	Input	VOUT_1.8V or VOUT_1.0V	**Host Sideband Bus Clock:** Bus clock used to strobe data into HUB device. When open drain, a pull-up resistor is required on the system motherboard.
HSDA	Input/ Output	VOUT_1.8V or VOUT_1.0V	**Host Sideband Bus Data:**I2C/I3C-Basic data. When open drain, a pull-up resistor is required on the system motherboard.

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Symbol	Type	I/O Level	Description
HSA	Input	GND	**Host Sideband Bus Device ID:** Address input to a hub or other client device to distinguish between identical devices in the I3C basic address range. Tied to GND, HSA has different resistor values on the motherboard to identify DIMM slot address. Refer to the SPD Hub spec for more information.
DQ[31:0]_A DQ[31:0]_B	Input/ Output	V_{DDQ}	**Data Input/Output:** Bidirectional data bus. If CRC is enabled via the mode register, then CRC code is added at the end of data burst. Any DQ from DQ0–DQ3 may indicate the internal V_{REF} level during test via mode register setting MR4 A4 = HIGH. Refer to the vendor-specific data sheets to determine which DQ is used.
CB[3:0]_A CB[3:0]_B	Input/ Output	V_{DDQ}	**ECC Check Bits Input/Output:**Bidirectional data bus.Only applicable on ECC SODIMM (SOEDIMM) or UDIMM(EUDIMM).
DQS[4:0]_A_t DQS[4:0]_B_t DQS[4:0]_A_c DQS[4:0]_B_c	Input/ Output	V_{DDQ}	**Data Strobe:** Output with read data, input with write data. Edge-aligned with read data, centered in write data. The data strobe DQS_t is paired with differential signals DQS_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR5 SDRAM only supports differential data strobe. It does not support single-ended strobe.
DM[3:0]_A_n DM[3:0]_B_n	Input	V_{DDQ}	**Input Data Mask:** DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a write access. DM_n is sampled on both edges of DQS. DM function is shared with TDQS on x8 devices. The function of DM_n is enabled by MR5:OP[5] = 1. Refer to Micron DDR5 component datasheet specification for further detail.
VIN_BULK	Supply		**External Power Supply:** 5V, 4.25V (min), 5.5V (max)
PWR_EN	Input		**PMIC Enable:** When this pin is HIGH, the PMIC turns on the regulator. When this pin is LOW, the PMIC turns off the regulator. This signal is connected to the PMIC's VR_EN pin.
V_{SS}	Supply		Ground
RFU			Reserved for future use. No on DIMM electrical connection is present.
NC			**No connect:** No internal electrical connection is present.
NF			**No function:** May have internal connection present, but has no function.

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Pin Assignments

288-Pin DDR5 UDIMM Front								288-Pin DDR5 UDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VIN_BULK	37	DQ20_A	73	CK0_A_c	109	V_{SS}	145	VIN_BULK	181	DQ22_A	217	CK1_A_c	253	V_{SS}
2	RFU	38	V_{SS}	74	V_{SS}	110	DQ5_B	146	VIN_BULK	182	V_{SS}	218	V_{SS}	254	DQ7_B
3	RFU	39	DQ21_A	75	RFU	111	V_{SS}	147	PWR_-GOOD	183	DQ23_A	219	RFU	255	V_{SS}
4	HSCL	40	V_{SS}	76	RFU	112	DQ8_B	148	HSA	184	V_{SS}	220	RFU	256	DQ10_B
5	HSDA	41	DQ24_A	77	V_{SS}	113	V_{SS}	149	RFU	185	DQ26_A	221	V_{SS}	257	V_{SS}
6	V_{SS}	42	V_{SS}	78	CK0_B_t	114	DQ9_B	150	V_{SS}	186	V_{SS}	222	CK1_B_t	258	DQ11_B
7	RFU	43	DQ25_A	79	CK0_B_c	115	V_{SS}	151	PWR_EN	187	DQ27_A	223	CK1_B_c	259	V_{SS}
8	V_{SS}	44	V_{SS}	80	V_{SS}	116	DM1_B_n	152	RFU	188	V_{SS}	224	V_{SS}	260	DQS1_B_c
9	DQ0_A	45	DM3_A_n	81	RFU	117	V_{SS}	153	V_{SS}	189	DQS3_A_c	225	RFU	261	DQS1_B_t
10	V_{SS}	46	V_{SS}	82	CA12_B	118	DQ12_B	154	DQ2_A	190	DQS3_A_t	226	RFU	262	V_{SS}
11	DQ1_A	47	DQ28_A	83	V_{SS}	119	V_{SS}	155	V_{SS}	191	V_{SS}	227	V_{SS}	263	DQ14_B
12	V_{SS}	48	V_{SS}	84	CA10_B	120	DQ13_B	156	DQ3_A	192	DQ30_A	228	CA11_B	264	V_{SS}
13	DQS0_A_c	49	DQ29_A	85	CA8_B	121	V_{SS}	157	V_{SS}	193	V_{SS}	229	CA9_B	265	DQ15_B
14	DQS0_A_t	50	V_{SS}	86	V_{SS}	122	DQ16_B	158	DM0_A_n	194	DQ31_A	230	V_{SS}	266	V_{SS}
15	V_{SS}	51	CB0_A	87	CA6_B	123	V_{SS}	159	V_{SS}	195	V_{SS}	231	CA7_B	267	DQ18_B
16	DQ4_A	52	V_{SS}	88	CA4_B	124	DQ17_B	160	DQ6_A	196	CB2_A	232	CA5_B	268	V_{SS}
17	V_{SS}	53	CB1_A	89	V_{SS}	125	V_{SS}	161	V_{SS}	197	V_{SS}	233	V_{SS}	269	DQ19_B
18	DQ5_A	54	V_{SS}	90	CA2_B	126	DQS2_B_c	162	DQ7_A	198	CB3_A	234	CA3_B	270	V_{SS}
19	V_{SS}	55	DQS4_A_c	91	CA0_B	127	DQS2_B_t	163	V_{SS}	199	V_{SS}	235	CA1_B	271	DM2_B_n
20	DQ8_A	56	DQS4_A_t	92	V_{SS}	128	V_{SS}	164	DQ10_A	200	ALERT_n	236	V_{SS}	272	V_{SS}
21	V_{SS}	57	V_{SS}	93	CS0_B_n	129	DQ20_B	165	V_{SS}	201	V_{SS}	237	CS1_B_n	273	DQ22_B
22	DQ9_A	58	CS0_A_n	94	V_{SS}	130	V_{SS}	166	DQ11_A	202	CS1_A_n	238	V_{SS}	274	V_{SS}
23	V_{SS}	59	V_{SS}	95	RESET_n	131	DQ21_B	167	V_{SS}	203	V_{SS}	239	DQS4_B_c	275	DQ23_B
24	DM1_A_n	60	CA0_A	96	V_{SS}	132	V_{SS}	168	DQS1_A_c	204	CA1_A	240	DQS4_B_t	276	V_{SS}
25	V_{SS}	61	CA2_A	97	CB0_B	133	DQ24_B	169	DQS1_A_t	205	CA3_A	241	V_{SS}	277	DQ26_B
26	DQ12_A	62	V_{SS}	98	V_{SS}	134	V_{SS}	170	V_{SS}	206	V_{SS}	242	CB2_B	278	V_{SS}
27	V_{SS}	63	CA4_A	99	CB1_B	135	DQ25_B	171	DQ14_A	207	CA5_A	243	V_{SS}	279	DQ27_B
28	DQ13_A	64	CA6_A	100	V_{SS}	136	V_{SS}	172	V_{SS}	208	CA7_A	244	CB3_B	280	V_{SS}

29	V_{SS}	65	V_{SS}	101	DQ0_B	137	DM3_B_n
30	DQ16_A	66	CA8_A	102	V_{SS}	138	V_{SS}
31	V_{SS}	67	CA10_A	103	DQ1_B	139	DQ28_B
32	DQ17_A	68	V_{SS}	104	V_{SS}	140	V_{SS}
33	V_{SS}	69	CA12_A	105	DQS0_B_c	141	DQ29_B
34	DQS2_A_c	70	RFU	106	DQS0_B_t	142	V_{SS}
35	DQS2_A_t	71	V_{SS}	107	V_{SS}	143	RFU
36	VSS	72	CK0_A_t	108	DQ4_B	144	RFU

173	DQ15_A	209	V_{SS}	245	V_{SS}	281	DQS3_B_c
174	V_{SS}	210	CA9_A	246	DQ2_B	282	DQS3_B_t
175	DQ18_A	211	CA11_A	247	V_{SS}	283	V_{SS}
176	V_{SS}	212	V_{SS}	248	DQ3_B	284	DQ30_B
177	DQ19_A	213	RFU	249	V_{SS}	285	V_{SS}
178	V_{SS}	214	RFU	250	DM0_B_n	286	DQ31_B
179	DM2_A_n	215	V_{SS}	251	V_{SS}	287	V_{SS}
180	VSS	216	CK1_A_t	252	DQ6_B	288	RFU

DDR5 SDRAM Thermal Characteristics

Symbol	Parameter/Condition	Value	Units	Notes
T_{OPER}	Normal Operating Temperature Range	0 to 85	°C	1
T_{STG}	DRAM Non-operating storage temperature	–20 to 90	°C	2

Notes:
1. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 - 85°C under all operating conditions.
2. Storage temperature is defined as the temperature of the top/center of the DRAM and does not reflect the storage temperatures of shipping trays.

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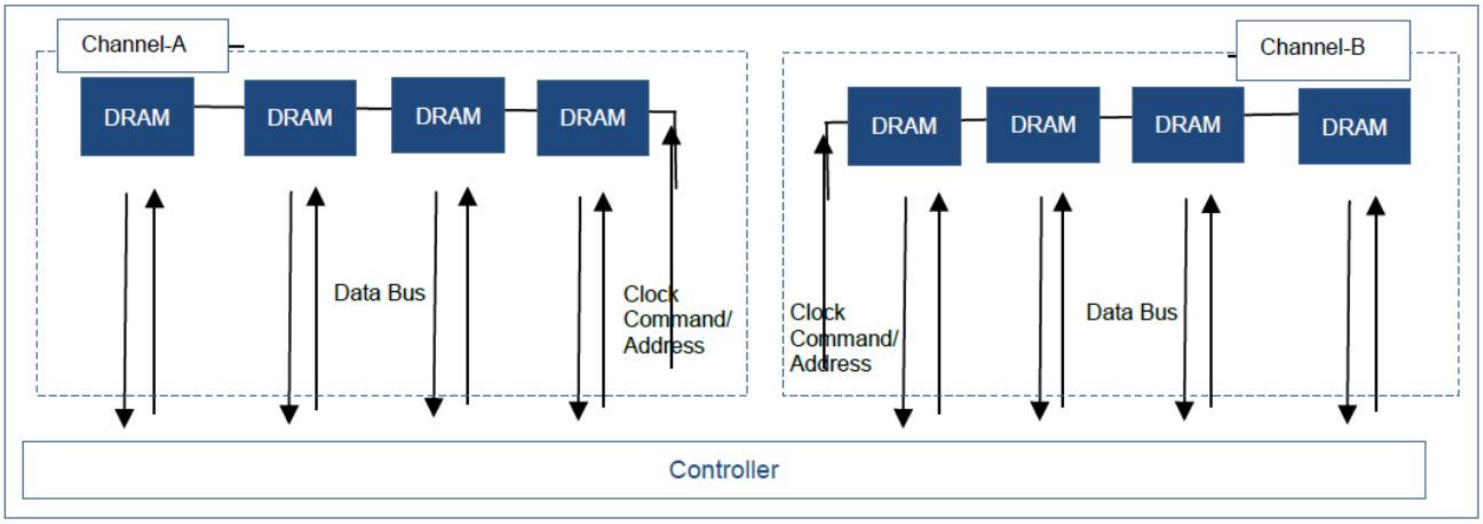
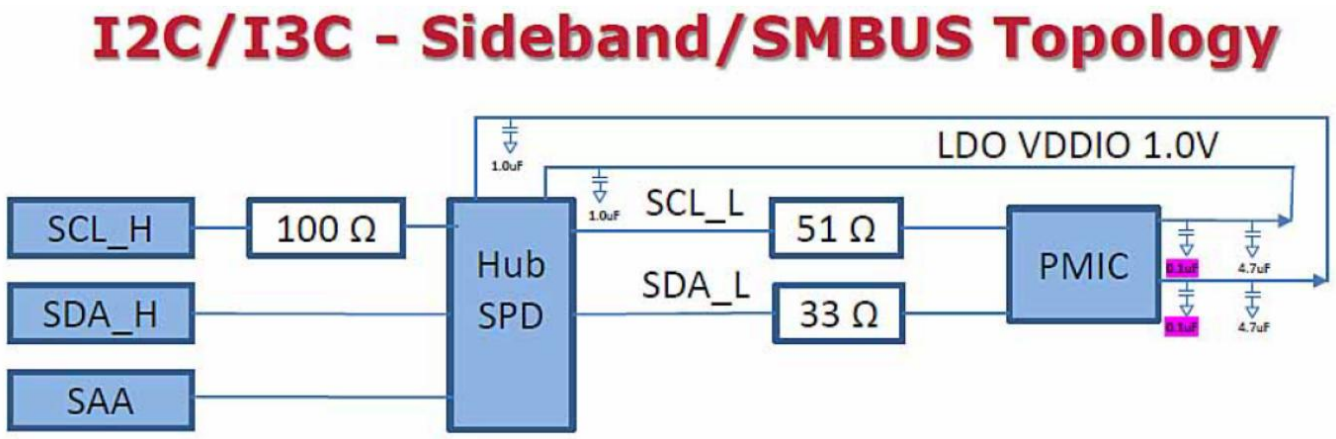
Functional Diagram





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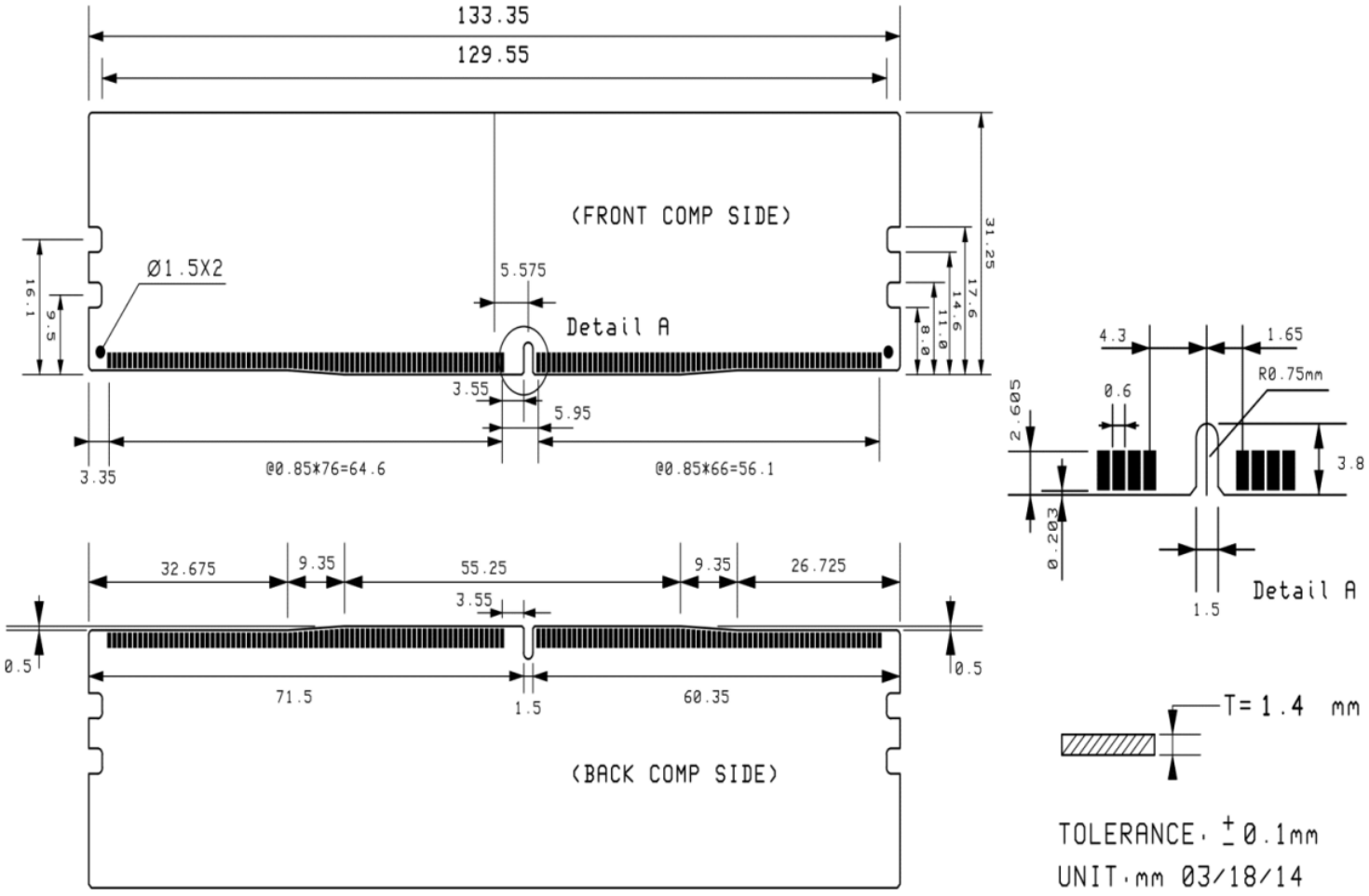
Module Dimensions



Notes:
1. All dimensions are in millimeters; MAX/MIN or typical (TYP) where noted.
2. Tolerance on all dimensions ±0.1 unless otherwise specified.
3. The dimensional diagram is for reference only.

Contact Information

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