Embedded Storage Solutions

（JUHOR）玖合

4GB / 8GB DDR3L-1600 SO-DIMM 1.35V

204pin PC3L-12800 DDR3L Unbuffered SO-DIMM Non-ECC

Description

JUHOR 4GB / 8GB are DDR3L 1600 Mbps SO-DIMM high-speed, memory module that use 16pcs 256M x 8bits，or 16pcs 512M x8bits

DDR3 SDRAM in FBGA package and a 2K bits serial EEPROM on a 204-pin printed circuit board.

JUHOR is a Dual In-Line Memory Module

and is intended for mounting into 204-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operation frequencies, programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

Features

- RoHS compliant products.
- JEDEC standard 1.35V(1.28V~1.45V) Power supply
  VDDQ= 1.35V(1.28V~1.45V)
- Data transfer rates: PC3L-12800
  Programmable CAS Latency:

CL= 11

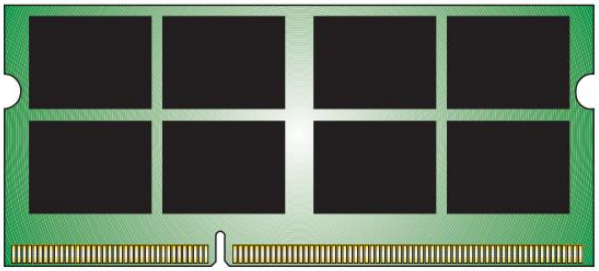
- 8 bit pre-fetch
- Burst Length (BL) switch on-the-fly BL8 or BC4
- Bi-directional Differential Data-Strobe
- On Die Termination, Nominal, Park, and Dynamic ODT
- Serial presence detect with EEPROM
  Asynchronous reset
- Anti - sulfur resistor used
- Operating Temperature(0°C ~ 85 °C)

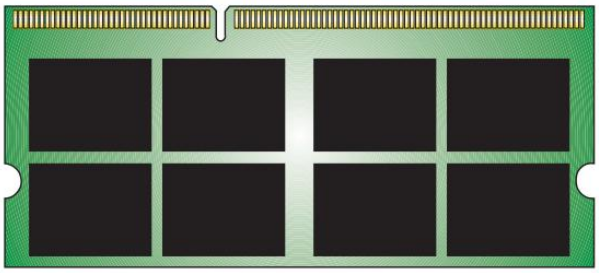
Pin Identification

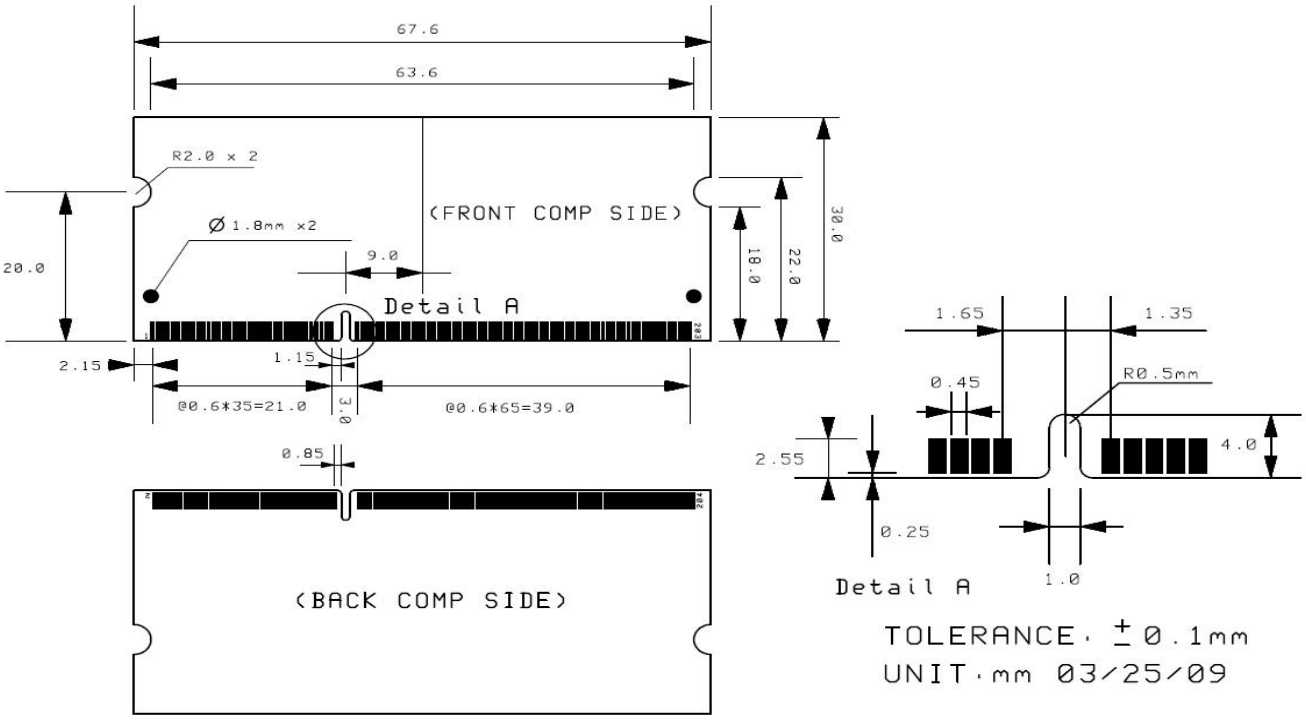
Symbol	Function
A0–A16, BA0~BA1	Address/Bank input
DQ0~DQ63	Bi-direction data bus.
DQS0_t–DQS7_t	Data Buffer data strobes
DQS0_c–DQS7_c	Data Buffer data strobes
CK0_t, CK1_t	Register clock input
CK0_c, CK1_c	Registert clocks input
ODT0 &ODT1	On-die termination control line
S_n [1:0]	DIMM chip selectst.
RAS_n[2]	Row address strobe
CAS_n[3]	Column address strobe
WE_n[4]	Write Enable
DM0~DM7	Data masks/high data strobes
VDD	Core power supply
VDDQ	I/O driver power supply
$V_{REF}CA$	Command/address reference supply
$V_{DD}SPD$	SPD EEPROM power supply
SA[1:0]	SPD and TS Address
SCL	I2C serial bus clock for EEPROM
SDA	I2C serial bus data for EEPROM
VSS	Ground
RESET_n	Set DRAMs Known State
VTT	DRAM I/O termination supply
ALERT_n	Register ALERT_n output
EVENT_n	SPD signals a thermal event has occurred
RFU	Reserved for future use

Please refer to the Pin assignments as follow

Dimensions (Unit: millimeter)







Note:1. Tolerances on all dimensions +/-0.15mm unless otherwise specified.

Pin Assignments

Front						Back					
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VREFDQ	69	DQ27	137	DQS4	2	VSS	70	DQ31	138	VSS
3	VSS	71	VSS	139	VSS	4	DQ4	72	VSS	140	DQ38
5	DQ0	73	CKE0	141	DQ34	6	DQ5	74	CKE1	142	DQ39
7	DQ1	75	VDD	143	DQ35	8	VSS	76	VDD	144	VSS
9	VSS	77	NC	145	VSS	10	/DQS0	78	A15*	146	DQ44
11	DM0	79	BA2	147	DQ40	12	DQS0	80	A14*	148	DQ45
13	VSS	81	VDD	149	DQ41	14	VSS	82	VDD	150	VSS
15	DQ2	83	A12,/BC	151	VSS	16	DQ6	84	A11	152	/DQS5
17	DQ3	85	A9	153	DM5	18	DQ7	86	A7	154	DQS5
19	VSS	87	VDD	155	VSS	20	VSS	88	VDD	156	VSS
21	DQ8	89	A8	157	DQ42	22	DQ12	90	A6	158	DQ46
23	DQ9	91	A5	159	DQ43	24	DQ13	92	A4	160	DQ47
25	VSS	93	VDD	161	VSS	26	VSS	94	VDD	162	VSS
27	/DQS1	95	A3	163	DQ48	28	DM1	96	A2	164	DQ52
29	DQS1	97	A1	165	DQ49	30	/RESET	98	A0	166	DQ53
31	VSS	99	VDD	167	VSS	32	VSS	100	VDD	168	VSS
33	DQ10	101	CK0	169	/DQS6	34	DQ14	102	CK1	170	DM6
35	DQ11	103	/CK0	171	DQS6	36	DQ15	104	/CK1	172	VSS
37	VSS	105	VDD	173	VSS	38	VSS	106	VDD	174	DQ54
39	DQ16	107	A10,/AP	175	DQ50	40	DQ20	108	BA1	176	DQ55
41	DQ17	109	BA0	177	DQ51	42	DQ21	110	/RAS	178	VSS
43	VSS	111	VDD	179	VSS	44	VSS	112	VDD	180	DQ60
45	/DQS2	113	/WE	181	DQ56	46	DM2	114	/S0	182	DQ61
47	DQS2	115	/CAS	183	DQ57	48	VSS	116	ODT0	184	VSS
49	VSS	117	VDD	185	VSS	50	DQ22	118	VDD	186	/DQS7
51	DQ18	119	A13*	187	DM7	52	DQ23	120	ODT1	188	DQS7
53	DQ19	121	/S1	189	VSS	54	VSS	122	NC	190	VSS
55	VSS	123	VDD	191	DQ58	56	DQ28	124	VDD	192	DQ62
57	DQ24	125	NC	193	DQ59	58	DQ29	126	VERFCA	194	DQ63
59	DQ25	127	VSS	195	VSS	60	VSS	128	VSS	196	VSS
61	VSS	129	DQ32	197	SA0	62	/DQS3	130	DQ36	198	/EVENT,NF
63	DM3	131	DQ33	199	VDDSPD	64	DQS3	132	DQ37	200	SDA
65	VSS	133	VSS	201	SA1	66	VSS	134	VSS	202	SCL
67	DQ26	135	/DQS4	203	VTT	68	DQ30	136	DM4	204	VTT

* This address might be connected to NC balls of the DRAMs (depending on density); either way they will be connected to the termination resistor.

4GB, 256Mx8 Module (2 Rank x8)
8GB, 512Mx8 Module (2 Rank x8)

- This technical information is based on industry standard data and tests believed to be reliable. However, Juhor makes no warranties, either expressed or implied, as to its accuracy and assume no liability in connection with the use of this product. Juhor reserves the right to make changes in specifications at any time without prior notice.

Operating Temperature Condition

Parameter	Symbol	Rating	Unit	Note
Operating Temperature	TOPER	0 to 85	°C	

Note: Operating Temperature is the case surface temperature on the center/top side of the DRAM.

Absolute Maximum DC Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on V_{DD} relative to Vss	VDD	-0.4 ~ 1.8	V	1,
Voltage on V_{DDQ} pin relative to Vss	VDDQ	-0.4 ~ 1.8	V	1
Voltage on any pin relative to Vss	VIN, VOUT	-0.3 ~ 1.8	V	1
Storage temperature	T_{STG}	-55~+100	°C	1,2

Note: 1. Stress greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

AC & DC Operating Conditions

Recommended DC operating conditions

Parameter	Symbol	Voltage	Rating			Unit	Notes
			Min	Typ.	Max		
Supply voltage	VDD	1.35V	1.28	1.35	1.45	V	1,2,3
Supply voltage for Output	VDDQ	1.35V	1.28	1.35	1.45	V	1,2,3
I/O Reference Voltage (DQ)	$VREF_{DQ}$(DC)	1.35V	0.49*VDD	0.50*VDD	0.51*VDD	V	4
I/O Reference Voltage (CMD/ADD)	$VREF_{CA}$(DC)	1.35V	0.49*VDD	0.50*VDD	0.51*VDD	V	4
AC Input Logic High	VIH(AC)	1.35V	VREF+135	-	VDD 2	mV	
AC Input Logic Low	VIL(AC)	1.35V	VSS 2	-	VREF–135	mV	
DC Input Logic High	VIH(DC)	135V	VREF+90	-	VDD	mV	
DC Input Logic Low	VIL(DC)	1.35V	VSS	-	VREF-90	mV	

Note: (1) Under all conditions VDDQ must be less than or equal to VDD.
(2) VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
(3) For DQ and DM, Vref = VrefDQ. For input ony pins except RESET#, Vref = VrefCA.
(4) The AC peak noise on VREF may not allow VREF to deviate from VREF(DC) by more than ±1% VDD (for reference: approx. ±12mV)

IDD Specification parameters Definition - 4GB (2 Rank x8)

Parameter	Symbol	DDR3L 1600 CL11	Unit
One bank; Active - Precharge	IDD0 [1]	208	mA
One bank; Active - Read - Precharge	IDD1	288	mA
Precharge Standby Current	IDD2N [2]	88	mA
Precharge standby ODT current	IDD2NT [1]	104	mA
Precharge Power-Down Current	IDD2P [2]	64	mA
Precharge Quiet Standby Current	IDD2Q [2]	64	mA
Active standby current	IDD3N [2]	168	mA
Active Power-Down Current	IDD3P [2]	80	mA
Burst Read Current	IDD4R [1]	512	mA
Burst write current	IDD4W [1]	504	mA
Burst refresh current (1x REF)	IDD5B [1]	1520	mA
Self refresh current: Normal temperature range (0–85°C)	IDD6N [2]	96	mA
Bank interleave read current	IDD7 [1]	968	mA
Maximum power-down current	IDD8 [2]	120	mA

Note: 1. One module rank in the active IDD/PP, the other rank in IDD2P.
2. All ranks in this IDD condition.
3.IDD current measure method and detail patterns are described on DDR3 component datasheet. Only for reference.

SERIAL PRESENCE DETECT SPECIFICATION (**Serial Presence Detect** only for reference)

Byte	Description	Function Supported	Serial PD Data Entry (Hexadecimal)	Note
0	Number of Serial PD Bytes Written during Production	112/256/176 Bytes	92	
1	SPD Revision	SPD Revision 1.3	13	
2	Key Byte/DRAM Device Type	DDR3-DRAM	0B	
3	Key Byte/Module type	SODIMM	03	
4	SDRAM Density and Banks	8 Banks, 4Gb	04	
5	SDRAM Address	15/11	21	
6	Reserve	1.35V Operable	02	
7	Module Organization	1 Rank x8	01	
8	Module Memory Bus Width	64bit Bus	03	
9	Fine Timebase (FTB) Dividend/Divisor	DDR3-Fine Timebase Dividend/Divisor	11	
10	Medium Timebase (MTB) Dividend	1ns	01	
11	Medium Timebase (MTB) Divisor	8	08	
12	SDRAM Minimum Cycle Time (tCKmin)	DDR3-Min SDRAM Cycle Time	0A	
13	Reserve	Reserved	00	
14	CAS latency, least Significant Byte	DDR3-CAS LATENCIES SUPPORTED	FC	
15	CAS latency, most Significant Byte	DDR3-CAS LATENCIES SUPPORTED	00	
16	Minimum CAS Latency Time (tAAmin)	13.125ns	69	
17	Minimum Write Recovery Time (tWRmin)	15ns	78	
18	Minimum RAS# to CAS# Delay Time (tRCDmin)	13.125ns	69	
19	Minimum Row Active to Row Active	DDR3-MIN ROW ACTIVE TO	30	

	Delay Time (tRRDmin)	ROW ACTIVE DELAY		
20	Minimum Row Precharge Delay Time (tRPmin)	13.125ns	69	
21	Upper Nibbles for tRAS and tRC	Refer to Byte 22,23	11	
22	Minimum Active to Precharge Delay Time (tRASmin), Least Significant Byte	35ns	18	
23	Minimum Active to Active/Refresh Delay Time (tRCmin), Least Significant Byte	48,75ns	81	
24	Minimum Refresh Recovery Delay Time (tRFCmin), Least Significant Byte	260ns	20	
25	Minimum Refresh Recovery Delay Time (tRFCmin), Most Significant Byte	260ns	08	
26	Minimum Internal Write to Read Command Delay Time (tWTRmin)	7.5ns	3C	
27	Minimum Internal Read to Precharge Command Delay Time (tRTPmin)	7.5ns	3C	
28	Upper Nibble for tFAW	Refer Byte 29	00	
29	Minimum Four Activate Window Delay Time (tFAWmin)	DDR3-MIN FOUR ACTIVE WINDOW DELAY	F0	
30	SDRAM Optional Features	DLL Off, RZQ/6, RZQ/7	83	
31	SDRAM Thermal and Refresh Options	DDR3-SDRAM DEVICE THERMAL REFRESH OPTIONS	01	
32	Module Thermal Sensor	Thermal Sensor	80	
33	SDRAM Device Type	Mono-Die	00	
34	Fine Offset for SDRAM Minimum Cycle Time (tCKmin)	1.071ns	00	
35	Fine Offset for Minimum CAS Latency Time (tAAmin)	13.125ns	00	
36	Fine Offset for Minimum RAS# to CAS# Delay Time (tRCDmin)	13.125ns	00	
37	Fine Offset for Minimum Row Precharge Delay Time (tRPmin)	13.125ns	00	

38	Fine Offset for Minimum Active to Active/Refresh Delay Time (tRCmin)	47.125ns	00	
39-40	Reserve	Reserve	00	
41	SDRAM Maximum Activate Count (MAC) Value		88	
42-59	Reserve	Reserve	00	
60-63	Module Type Specific Section,	-	0F 11 41 00	
64-117	Reserve	-	00	
117-118	Module ID: Module Manufacturer's JEDEC ID Code	JUHOR	08 75	
119	Module ID: Module Manufacturing Location	-	02	
120-121	Module ID: Module Manufacturing Date	-	-	
122-125	Module Serial Number	-	-	
126-127	SPD Cyclical Redundancy Code	-	63 A2	
128-145	Module Part Number			
146-147	Module Revision Code	-	00 10	
148-149	DRAM Module Manufacturer's JEDEC ID Code	-	00 00	
150-175	Manufacturer's Specific Data	-	-	
176-255	Open for customer use	-	-	

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